REMARKS

Summary of the Office Action

Claims 17 and 18 were objected to because of informalities.

Claims 1-20 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

Summary of Applicant's Response

Applicant has amended claims 17 and 18 to correct for the informalities.

Applicant respectfully traverses the rejections under 35 U.S.C. § 112, first paragraph.

Reply to Rejections Under 35 U.S.C. § 112, First Paragraph

Applicant respectfully traverses the Examiner's rejection of claims 1-20 under 35 U.S.C. § 112, first paragraph, as failure to comply with the enablement requirement. Applicant submits that the claimed invention is described in the specification in such full, clear, concise and exact terms as to enable persons skilled in the art to make and use the claimed inventions.

First, applicant respectfully traverses the statement in the Office action that "the specification does not explain what circuit includes the sourcing circuit with a substantially inductive impedance characteristic" (Office action, page 2). Such circuit is illustrated in FIG. 1 as "inductive sourcing circuit 110" (specification, page 5, line 27) that "may include

any circuit configuration that exhibits a substantially inductive frequency characteristic (*i.e.*, impedance that increases as frequency increases) and is suitable for providing current (e.g., such as the circuitry shown in FIG. 2)" (specification, page 6, lines 9-13).

Furthermore, applicant directs the Examiner to FIG. 2, which shows one embodiment of such an inductive sourcing circuit. In particular, "resistor 211 and transistor 212 form a well known drain load that acts as a sourcing circuit with an inductive impedance" (specification, page 9, lines 31-33). The combination of resistor 211 and transistor 212 forms a "synthetic circuit element" (specification, page 10, line 8) that mimics an inductor.

As an example of what was known in the prior art, applicant directs the Examiner's attention to the illustrative sourcing circuit with a substantially inductive impedance characteristic discussed by Sackinger et al. in "A 3GHz, 32dB CMOS Limiting Amplifier for SONET OC-48 Receivers", <u>IEEE International Solid-State Circuits Conference</u>, 2000 (hereinafter "the Sackinger article"). The Sackinger article was previously identified by the applicant in the Information Disclosure Statement submitted on October 29, 2003 and a copy is attached herewith in Appendix A for the Examiner's convenience. In particular, applicant directs the Examiner's attention to the first full paragraph in column two of page 158 and FIG. 9.5.4(b) on page 159 of the Sackinger article. The principles of the sourcing circuit discussed in the Sackinger article are well-known to those skilled in the art. As such, those skilled in the art would be able to make and/or use a

sourcing circuit with a substantially inductive impedance characteristic without undue experimentation.

Applicant notes that independent claim 1 of U.S. Patent Application No. 10/172,874 (hereinafter "the '874 application"), which issued as U.S. Patent No. 6,670,850 (hereinafter "the '850 patent") on December 30, 2003 and from which the present application claims priority, also recites "a sourcing circuit with a substantially inductive impedance characteristic". Since the present application is a continuation of the '874 application, the specification of the '874 application is identical to that of the present application.

As discussed in the specification, "actual inductors may be used in sourcing circuit 110 if desired" (specification, page 10, lines 5-6) but "as is well known in the art, actual inductors are somewhat difficult to fabricate and tend to use relatively large amounts of die space" (specification, page 10, lines 11-13). By using the combination of resistor 211 and transistor 212 as illustrated in FIG. 2 to form "a sourcing circuit with a substantially inductive impedance characteristic" (claims 1, 13, and 19), "it is possible to reduce die size, power consumption, and manufacturing time" (specification, page 10, lines 14-16).

As such, "inductive sourcing circuit 110 provides at least two important benefits" (specification, page 6, lines 28-29) to amplifier circuit 100. First, "it acts as a high impedance element at high frequencies causing an increasing portion of the output signal produced by amplifier 100 to pass through the load" (specification, page 6, lines 29-32). And

second, "it prevents high frequency signals generated by modulation circuit 130 from being introduced onto a power plane (not shown) coupled to inductive sourcing circuit 110" (specification, page 7, lines 7-10).

Accordingly, applicant submits that the claim limitation reciting "a sourcing circuit with a substantially inductive impedance characteristic" in claims 1, 13, and 19 is described in the specification as filed, and respectfully requests that the §112, first paragraph, rejections be withdrawn.

Conclusion

In view of the above amendments and remarks, applicant respectfully submits that the present application is in condition for allowance.

Respectfully submitted,

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First Edition

February 2000

IEEE Catalog Number 00CH37056

Publisher: John H. Wuorinen, Castine, ME 04421

2000 IEEE International Solid-State Circuits Conference

DIGEST OF TECHNICAL PAPERS

PRINTED IN THE UNITED STATES OF AMERICA
by The J. S. McCarthy Co.
Augusta, Maine

VOLUME 43

IEEE Cat. No. 00CH37056
ISBN 0-7803-5853-8 Softbound
ISBN 0-7803-5854-6 Casebound
ISBN 0-7803-5855-4 Microfiche
ISBN 0-7803-5856-2 CD-ROM
Library of Congress Number 81-644810
ISSN 0193-6530

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Conference Information:

TA 9.5 A 3GHz, 32dB CMOS Limiting Amplifier for SONET OC-48 Receivers

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Figure 9.5.1 shows an optical receiver front-end for SONET OC-48 (2.5Gb/s). The limiting amplifier (LA) receives a small non-return to zero (NRZ) voltage signal (e.g., $8mV_{pp}$) from the transimpedance amplifier (TIA) and amplifies it to a level (e.g. $250mV_{pp}$) sufficient for the reliable operation of the clock and data recovery (CDR) circuit. The noise contribution of the LA must be small compared to that of the TIA so that the overall bit error rate and sensitivity are not affected adversely. Currently, commercial 2.5Gb/s SONET systems are composed of several discrete chips (TIA, LA, CDR, demultiplexer, clock synthesizer, multiplexer, laser driver, etc.) implemented in GaAs and more recently silicon bipolar technology. The future trend, however, is to integrate most of the front-end together with the digital framer on a single CMOS chip. Furthermore, the integration of multiple 2.5Gb/s channels on a single CMOS chip is desirable for wavelength division multiplexing (WDM) application. CMOS amplifiers for optical receivers and related applications with bandwidths up to 2.1GHz are recently reported [1,2,3]. This CMOS limiting amplifier with improved bandwidth (3GHz) and noise figure (16dB) is suitable for 2.5Gb/s SONET receivers. Power dissipation is 53mW and the chip is fabricated in a standard 2.5V, 0.25μm CMOS technology. This result is achieved with: (i) Inverse scaling to increase gain-bandwidth and reduce power dissipation while keeping noise and offset voltage low and (ii) active inductors to increase gain-bandwidth and improve gain stability. The active area of the amplifier is $0.03mm^2$, less than 10% that of a comparable design with spiral inductors.

Figure 9.5.2 shows the block diagram of the CMOS limiting amplifier. It consists of four gain stages (A_1 - A_4) which provide a total gain of 34dB and a buffer stage (gain = -2dB) to drive the on-chip CDR load of 0.1pF. The gain stages are scaled so the transistor widths in the driven stage are half the size of those in the driving stage. The relative transistor sizes are marked as 1x, .., 8x in Figure 9.5.2. Figure 9.5.3 shows circuit details of the individual stages. The first stage (A_1) is a common-gate differential pair providing low impedance input. Its bias currents (I_{BI}) are controlled so the input impedance is 50Ω. Stages A_2, A_3, A_4 are common-source differential pairs, and the buffer stage is implemented with two source followers. An offset compensation circuit controls the current I_{OS} in the input stage so the dc amplifier output voltage is zero. This paper discusses the implementation of the amplifier core drawn with solid lines in Figure 9.5.2.

The gain-bandwidth of each stage is given by the ratio g_m/C_{tot} where g_m is the transconductance and C_{tot} is the total load capacitance of the stage. The latter consists of the stage output capacitance, the wiring capacitance, and the next-stage input capacitance. In the absence of scaling, these capacitances for the first stage (A_1) are 100fF, 20fF, and 180fF, respectively, i.e., a substantial fraction is due to the next-stage input capacitance which includes a Miller component. If the second stage is scaled down by a factor 2, the total capacitive load reduces to (100+20+180/2)fF = 210fF and the bandwidth of the first stage increases by about 43%. Successive downscaling, as shown in Figure 9.5.2, increases the bandwidth of all stages. Note that inverse scaling is applicable here because only a small on-chip capacitance of the CDR needs to be driven, while a large input capacitance can be tolerated at the 50Ω input. The output load capacitance of the 4th stage is 14fF given by the CDR load and the capacitance transformation ratio of the source follower (≈1 : 7). The maximum input capacitance of the amplifier is limited to about 250fF to meet the input return loss (S_{11}) specifications. The capacitance ratio of 250fF : 14fF leads to the optimum scale factor of 1/2 per stage used in this design. Furthermore, as a result of inverse scaling the power consumption of stages A_2 - A_4 is reduced significantly without compromising the low noise and low offset of the amplifier, which are determined primarily by the large input stage A_1.

The amplifier bandwidth is further extended by the use of inductive loads in every gain stage. This technique moves each stage pole to a higher frequency by partly tuning out its capacitive load. For large inductances, undesired peaking occurs in the frequency response. The bandwidth can be extended by about 70% before peaking occurs. Inductive loads can be implemented with spiral inductors or active inductors [4] (Figure 9.5.4). It is difficult to design spiral inductors with high inductance (e.g. 20nH) and keep the self-resonance well outside the passband (>> 3GHz). Furthermore, eight spiral inductors consume a large area and prevent a compact floorplan. In contrast, active inductors are small and operate up to about $f_T/2$ (f_T≈25GHz at V_{GS}=0.9V in this technology). However, the large dc voltage drop across the conventional active inductor presents a problem at low supply voltages. Our solution is to bias the resistors of the active inductors one nMOS threshold voltage (note that this threshold voltage is increased by the back-gate effect) above V_{DD} reducing the voltage drop across the inductor by about half (Figure 9.5.4). Since no current is drawn from this bias voltage (V_{BH}), it can be generated on-chip with a capacitive voltage converter. A further advantage of the active inductor load is that the amplifier dc gain becomes process insensitive, because the geometrical ratio of nMOS transistors M1 and M2 determines the gain (Figure 9.5.3).

The chip micrograph shows the inversely scaled stages (Figure 9.5.5). Some of the biasing transistors and poly resistors are covered by metal and are not visible. The ouput of the LA drives a 50Ω test buffer which presents the same capacitive load as the CDR and can drive a 50Ω load for testing purposes. This 50Ω test buffer was also integrated separately to determine its dc gain (-5.3dB) and verify its bandwidth. An eye diagram measured at 2.5Gb/s and a $2mV_{pp}$, 2^{31}-1 PRBS input signal is shown in Figure 9.5.6. The eye is measured single-endedly through the 50Ω test buffer. The available input-referred rms noise is 155μV corresponding to $2.2mV_{pp}$ sensitivity at 10^{-12} bit error rate (BER). Additional performance data is listed in Figure 9.5.7.

Acknowledgments:
The authors thank P. Kinget, H. Kim, P. Larsson, and M. Loinaz for discussions.

References:

[1] Tanabe, A. et al., "A Single Chip 2.4Gb/s CMOS Optical Receiver IC with Low Substrate Crosstalk Preamplifier," ISSCC Digest of Technical Papers, pp. 304—305, Feb. 1998.
[2] Savoy, J. and Razavi, B., "A CMOS Interface Circuit for Detection of 1.2Gb/s RZ Data," ISSCC Digest of Technical Papers, pp. 278—279, Feb. 1999.
[3] Yoon, T. and Jalali, B., "Front-End CMOS Chipset for Fiber-Based Gigabit Ethernet," Symposium on VLSI Circuits Digest of Technical Papers, pp. 188—191, June 1998.
[4] Hara, S. et al., "Broad-Band Monolithic Microwave Active Inductor and its Application to Miniaturized Wide-Band Amplifiers," IEEE Trans. on Microwave Theory and Techniques, pp. 1920—1924, Dec. 1988.

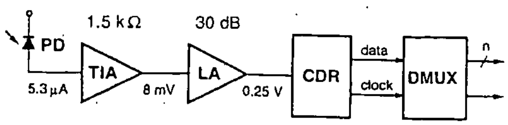

Figure 9.5.1: 2.5Gb/s SONET receiver front-end block diagram.

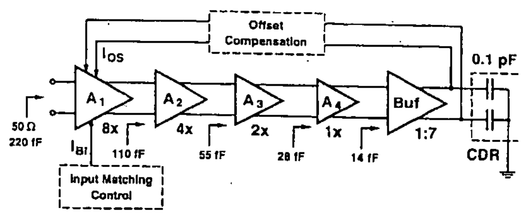

Figure 9.5.2: 3GHz CMOS limiting amplifier block diagram.

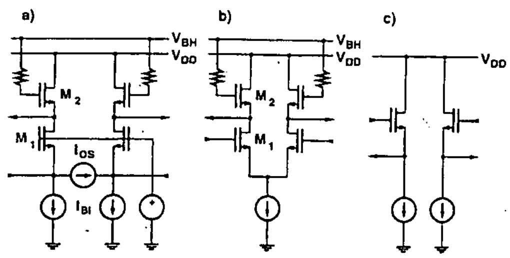

Figure 9.5.3: Amplifier circuits: a) first gain stage, b) gain stages 2-4, c) buffer stage.

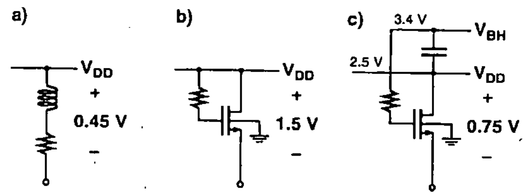

Figure 9.5.4: Inductive loads: a) spiral inductor and resistor, b) conventional active inductor, c) low voltage-drop active inductor.

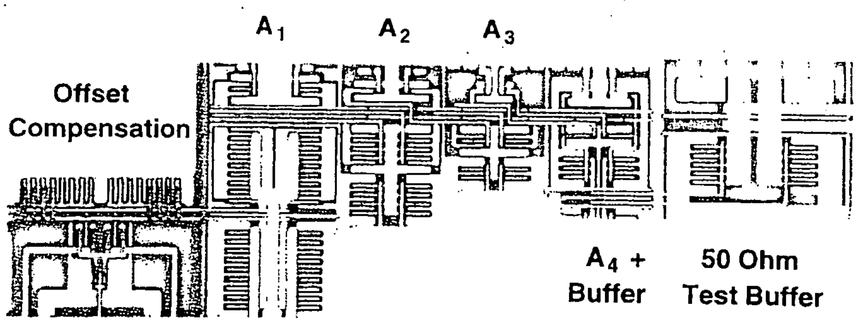

Figure 9.5.5: Chip micrograph.

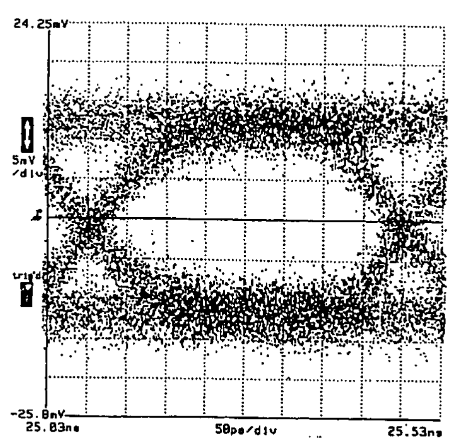

Figure 9.5.6: Eye diagram with a 2.5Gb/s, 2mVpp PRBS input signal.

Parameter	Value
CMOS Technology	2.5 V, 0.25 μm
Active area	0.03 mm^2
Bandwidth (−3 dB)	3 GHz
DC Gain (differential)	32 dB
Group Delay (1 GHz)	125 ps
Group Delay Variation (1 – 3 GHz)	15 ps
Rise/Fall Time (20 % – 80 %)	106 ps
Input Dynamic Range (p-p)	2 mV - 2 V
AM to PM Conv. (5 mV$_{pp}$ – 2 V$_{pp}$)	< 10 ps
Available Input Noise (rms)	155 μV
Noise Figure (1 GHz)	16 dB
Input Return Loss (2 GHz)	19 dB
Input Return Loss (3 GHz)	17 dB
Power Dissipation	53 mW

Figure 9.5.7: Measured performance.